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NOVEL FLIPFLOP DESIGN USING GDI TECHNIQUE

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ABSTRACT:

Low power, low space, and high-speed design of flip flops using fewer transistors are discussed in this study. When designing digital circuits, the Modified Gate Diffusion Technique (M-GDI) is an alternative to CMOS and PTL (Pass Transistor Logic). As a result, the size of the circuit and the amount of power dissipation are both reduced. A thorough evaluation of existing designs of True SinglePhase Clocking Flip-Flops with positive edge triggers is performed. Minimize transistor size and power dissipation as compared to the design of real single-phase clocking flip-flop (FF) transistors in this study Master-slave logic is used in the design.

INTRODUCTION:

Digital designs of all types heavily rely on the fundamental storage device known as the flip-flop (FF). FF-rich modules like register file, shift register, and first in first out (FIFO) are often used in digital architectures nowadays. FFs provide a substantial amount of chip space and power consumption to the overall architecture of the overall system. Additionally, novel FF designs are needed to meet specific application requirements like as fast speed, low power, and low voltage.

VLSI systems, such as digital signal processing (DSP) processors and microprocessors, frequently include adders as circuit parts. Many additional operations, such as subtraction, have its foundation in this concept.University of Kakinada's Engineering College (A)University of Kakinada, Jawaharlal Nehru Technological University Aishunarayan25@gmail.com is her email address.Adding, subtracting, and multiplying and dividing. Adders are commonly found along the critical path of digital systems, where they have an impact on the overall system performance.

Because of this, it is becoming more and more vital to improve the performance of the adder. Low-power microelectronics research has being stepped up due to the rapid expansion of portable devices like laptops.

It's because battery technology hasn't progressed at the same pace as microelectronics technology. For the mobile systems, there is only a limited quantity of electricity. As a result, a focus on low power design has emerged [4]. Most computing-intensive tasks, such as multimedia processing and DSP, may now be implemented in hardware thanks to advancements in VLSI technology. It's no surprise that experts are working hard to reduce silicon area, increase performance, and extend battery life of

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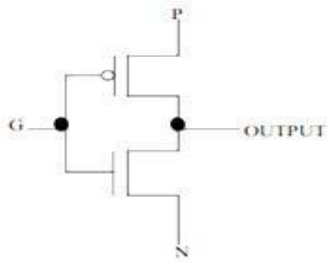
portable electronic devices as demand grows and popularity rises. The complete adder architecture is critical to digital computing. When designing a complete adder, the design requirements might be several [5].Transistor count, which is one of the features, influences the system complexity of arithmetic circuits like multiplier, Arithmetic Logic Unit (ALU), etc. For complete adders, speed and power consumption are also critical considerations. They are, nevertheless, in opposition to one another.

Consequently, to achieve optimal design tradeoffs, the power delay product or energy consumption per operation has been introduced Proper selection of logic types can improve digital circuit performance.

One feature of a performance may be favoured at the expense of others under different reasoning styles. Although the logic types accomplish the same function, the methods of computing intermediary nodes and the number of transistors are different [6]. Static CMOS, dynamic circuits, transmission gates and GDI logic are among the several complete adder architectures studied in the literature [7–12].

CMOS adders with complementary pull-up PMOS and pull down NMOS networks require 28 transistors to provide sum and carry outputs. When compared to CMOS, PTL uses less transistors per function implementation.



As a result, the total capacitance may be reduced, allowing for higher speeds and lower power consumption. Because of threshold voltage loss at both input and output in a PTL-based system, the output voltage varies.

Leakage power consumption should be decreased as well, in addition to the switching power. One of the most extensively used FFs nowadays is a TGFF, which is a transmissiongate-based FF (TFG). To reduce clock signal burden, genuine single-phase clocking (TSPC) FF designs have been created.

Circuit simplification is the most common way to do this.

This type of FF is more widely used than the traditional transmission gate (TG) and master-slave-based variants because of the simplicity and fast speed of pulse triggering. In response to a clocking pulse, a flip-flop electrical circuit records the logical state of one or more data input signals. In an effort to reduce clock signal stacking, true single-phase clocking (TSPC) FF designs have been developed.Disentanglement of circuits is the most common method of accomplishing this. As an alternative to using the TG-based hook, cross-coupled set–reset (SR) locks are used. Static logic and complementary pass-transistor logic (CPL) are used in an SR-latch (SRFF)[1] architecture. TSPC procedures are used in this architecture to reduce the clock signal load. The Gate Diffusion Method in a new form (M-GDI) In addition to CMOS and PTL, there are additional techniques for designing digital circuits that can improve performance (Pass Transistor Logic). As a result, the size of the circuit and the amount of power dissipation are both reduced. A thorough evaluation of existing designs of True

SinglePhase Clocking Flip-Flops with positive edge triggers is performed.

Minimize transistor size and power dissipation as compared to the design of real single-phase clocking flip-flop (FF) transistors in this study The design is based on a master–slave logic.

II.ADVANCED GRAPHIC IMPLEMENTATION

Fig. 1 depicts the simplest GDI cell. 1. In spite of the fact that it looks like a CMOS inverter, the source/drain diffusion inputs of each transistors are unique. In

source and drain diffusion input in a standard inverter circuit

The VDD and GND potentials of PMOS and NMOS transistors are always connected. GDI's diffusion terminal, on the other hand, serves as an external input. Threshold voltage loss is a major problem with GDI gates. The gate's performance suffers as a result of the reduced current drive.

Fig.1: The simplest GDI cell.

This technique relies on the employment of just a single cell in order to work. For example, the GDI cell has G (the common gate input of the two transistors), P (the input to the outer diffusion node of PMOS transistor) and N (the common gate input of NMOS transistors) (input to the outer diffusion node of the PMOS transistor). The Out node (common diffusion of both transistors) can be utilised as either an input or output port, depending on the circuit design. The GDI cell's construction is similar to that of a CMOS switch. The PMOS source is coupled to VDD, whereas the NMOS source is grounded in a CMOS inverter. However, in a GDI cell, this may not be the case.

inevitably happen. The two have several significant distinctions. The three sources of information used inThere is just one GDI in particular.

NMOS and PMOS gate common inputs are designated as G.

Second, the NMOS source/drain accepts N-input

PMOS source/drain is 3) P-input

But when linked in series, the inverters in the buffers raise both the transistor count and the static power consumption. When a voltage decrease is expected, low threshold transistors will be used, while high threshold transistors will be used in the inverters. Despite the fact that this hybrid threshold voltage approach reduces power consumption, it causes a bottleneck during the transistor manufacture process. The MOS transistor is configured as a diode and eight more transistors are used to provide full swing. As a traditional swing restoration buffer, it helps to reduce static power dissipation, but the difficulty of ULPD manufacturing must still be taken into mind. So date, the only ways to get a complete adder output swing have been to increase the number of transistors or increase the amount of electricity used (use of buffers). In order to build full swing at the gate level like AND, OR, XOR, etc. a generic technique is needed. Next this effort to build three full swing gates, a thorough explanation of the suggested gates is given in the following section.

As a result, the GDI cell provides two additional input pins, making it more adaptable than the CMOS design. A GDI cell has three inputs: G (the NMOS and PMOS common gate input), P (the PMOS source/drain input), and N (the NMOS source/drain input). To N and P, respectively, NMOS and PMOS wires are joined in large swaths.

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Basic GDI Cell Logical Functions (Table 1)

As a result, the GDI cell provides two additional input pins, making it more adaptable than the CMOS design.

design. G (common gate input of NMOS and PMOS), P (input to the source/drain of the PMOS) and N (input to the source/drain of the NMOS) are the three inputs of a GDI cell. To N and P, respectively, NMOS and PMOS wires are joined in large swaths. Based on the input data, GDI logic [8] implements several logic functions as shown in Table 1. As a result, the GDI approach may be used to create a wide range of logic functions at a lower power consumption and higher speed than standard CMOS architecture.

II. GDI IN D-FF MODIFIED

Using a GDI cell in a D-FilpFlop reduces transistor area compared to the LRFF method [1].

The number of transistors drops to 16 as a result of this. as seen in the GDI-based flipflop circuit schematic in fig.2.

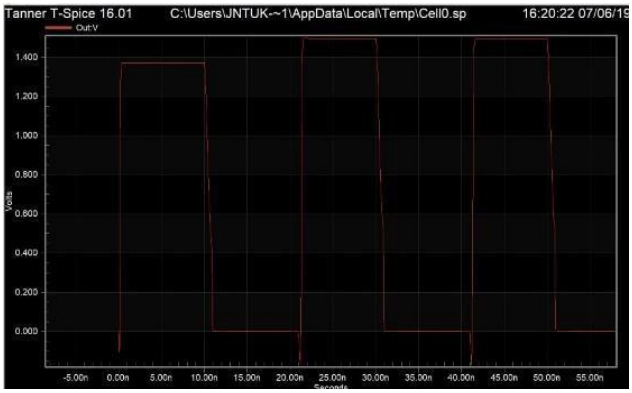


fig.2 circuit diagram of GDI based flipflop.

fig.3: OUTPUT WAVEFORM GDI based flipflop.

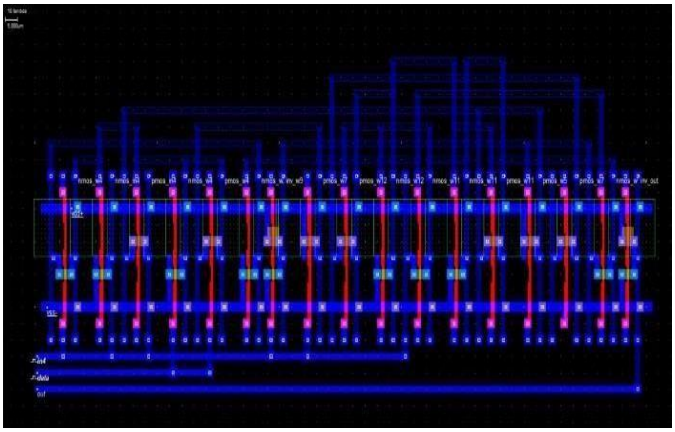


Fig.4.layout modified GDI based

CONCLUSION:

Proliferation delays decrease and static power dissipation increases when innovation is reduced, according to the results. As a result, this M GDI flip-flop has the least amount of power delay (PDP) and hence provides the best performance. It is possible to get rid of the clock skew that is generated by different clock phases with this type of circuit, and the off-chip production of clock signals saves chip area and power consumption. In addition, it may be used in a variety of applications, including level converters, microchips, and timing framework counters.

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