ISSN : 2347 - 2243

Indo - American Journal of Life Sciences and Biotechnology

www.iajlb.com
Email : editor@iajlb.com or iajlb.editor@gamil.com

Indo-American Journal of Life Sciences and Biotechnology

Vol.10, Issue.2, June 2022

Design and analysis of high-performance CMOS5-2com pressor with 58 transistors

ShaikHaseenaBegum1, G. VijayaKiran2

ABSTRACT: Compressors are the building blocks of CMOS multipliers' partial product reduction stage. The CMOS 5-2 compressor is given a new design with 58 transistors, the lowest device count ever reported for such a circuit. MICROWIND 3.5 is used to run 65nm Verilog simulations on 65nm technology. The circuits were first built using the DSCH 3.5 Tool and the Verilog file was generated. The suggested 5-2 compressor has much better power delay performance than previously proposed techniques, according to simulation findings.

IndexTerms–CMOSLayout, 58 Transistors, Low-Power Compressor

Introduction:

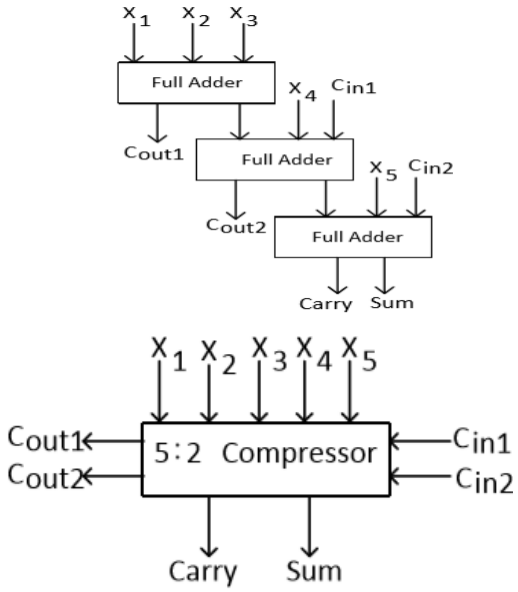
Adding and subtracting are the two most common arithmetic operations. Operations like multiply and Accumulate unit (MAC), convolution and FFT (Fast Fourier Transform). Due to the fact that DSP systems' execution times are heavily influenced by multiplication, faster multipliers are required.

The need for a high-speed, low-power electronics system is becoming more and more prevalent. For this reason, VLSI experts have been working for decades to create a system that is both quick and efficient. [1] A high-speed (m:n) compressor is a processing unit that receives m inputs and produces n output [1]. [1] There is a wide range of applications for high speed compressors, such as digital signal processors (DSPs), general-purpose micro-processors, 3-D graphics applications (e.g. stereoscopic), motion estimation accelerators, and more [2]-[7]. Some of the aforementioned uses require a multiplier. Compressors are used in multipliers to reduce the number of operands when the first stage's partial products are added [1], [4]. As a result, high-speed, low-power and area-efficient compressors are used in a variety of multipliers, including Vedic multiplier, Wallace tree multiplier and Array multiplier. Compressors with a capacity of 4-2 have been developed by VLSI designers, and this particular model is one of the most widely used.

1PGStudent,Dept.ofECE(VLSI&ES), SSNEngineeringCollege,Ongole,AP,India.
2AssociateProfessor,Dept.ofECE,SSNEngineeringCollege,Ongole,AP,India.

quick digital computing circuits because of their connectivity and simple form.

Compressor trees, which often use 4-2 and 5-2 compressors as construction components, are an effective way to accomplish partial product reduction. The overall performance of the multiplier is directly influenced by improving the compressor cell. The concept of a high performance 16 16 bit multiplier using a 5- 2 compressor was first presented in [2], but no



details on transistor-level implementation were published. New designs for the 5-2 compressor have been proposed in a number of subsequent papers [3–8]. By way of example, we'll show how we can reduce the transistor count on an existing design while still providing great performance. Additionally, the new circuit is compared to existing designs in a comparative analysis.

5-2 Compressor functionalityCompressors are crucial to the multiplication process since they are utilized to acquire incomplete products. All columns of the partial product are added in parallel without relying on the previous carry, which is the primary concept of a compressor's basic design principle. A 3:2 compressor is an early example of a full adder circuit, which is the earliest type of compressor. The 4:2 compressors [15] are the next generation of sophisticated compressors. They reduce four partial products into two, resulting in a higher compression ratio than the 3:2. The 5:2 compressor is a tertiary compressor after the 4:2 compressor. Figure 1 depicts the overall structure (a)

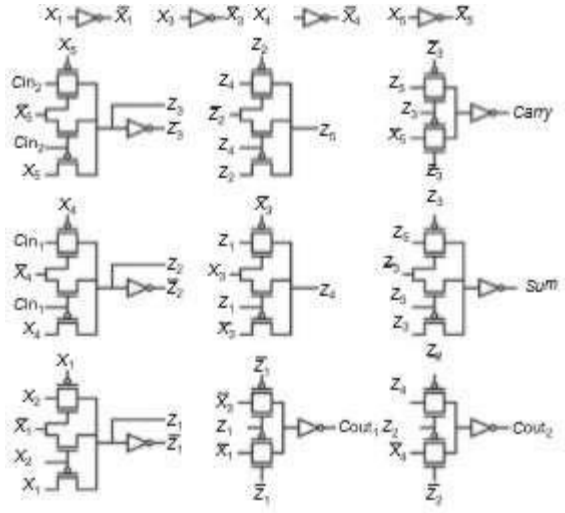
Fig1(a):Basic5:2Compressorstructure [17]

Out of the seven inputs,fiveare direct inputs X1,X2,X3,X4andX5andtwoarecarryinputsCin1

Cin2 from an earlier stage. Additionally, there are four outputs: two carry out bits (Cout1, Cout2) to the next step and two sum and carry bits (Sum and Carry). Fig. 1 shows a typical representation of 5:2 using three cascaded full adders (b).

Fig.1(b):5:2withFull Adders[17]

The operation of Fig.3 can be explained with respectto Fig. 1. The regular implementation of



5:2 is withXOR-

$$\mathrm{Sum} = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_5 \oplus C_{in1} \oplus C_{in2} \quad (1)$$

$$\mathrm{Sum} = \left\{ \begin{array}{l} \left\{ \left[(X_1 \oplus X_2) X_3' + X_3 (X_1 \oplus X_2)' \right] \oplus \\ \left[(X_4 \oplus X_5)' C_{in1} + C_{in1}' (X_4 \oplus X_5) \right] \end{array} \right\} C_{in2}' + \left\{ \begin{array}{l} \left\{ \left[(X_1 \oplus X_2) X_3' + X_3 (X_1 \oplus X_2)' \right] \oplus \\ \left[(X_4 \oplus X_5)' C_{in1} + C_{in1}' (X_4 \oplus X_5) \right] \end{array} \right\}' C_{in2} \quad (2)$$

$$\mathrm{Carry} = \left[(X_1 \oplus X_2 \oplus X_3) \oplus (X_4 \oplus X_5 \oplus C_{in1}) \right] C_{in2} + (X_1 \oplus X_2 \oplus X_3) \left[(X_1 \oplus X_2 \oplus X_3) \oplus (X_4 \oplus X_5 \oplus C_{in1}) \right]' \quad (3)$$

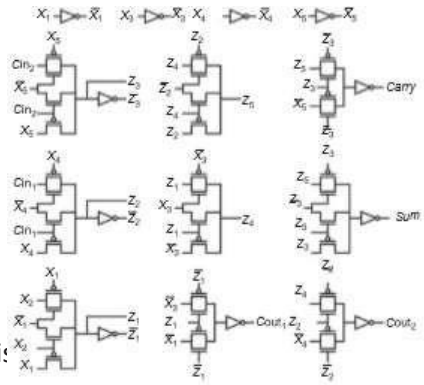
$$C_{out1} = X_1 X_2 + X_2 X_3 + X_1 X_3$$

$$C_{out2} = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) C_{in1} + (X_1 \oplus X_2 \oplus X_3 \oplus X_4)' X_4 \quad (4)$$

XNORblocksandthesumandcarryexpressionsare givenbythefollowingequations[17].

I. PROPOSEDCIRCUIT

Figure 2a depicts a block diagram of the proposed 5-2 compressor. Generalized schematics for the blocks are presented in Figures 2 and 3; the XOR and MUX blocks are depicted in Fig. 2, respectively. Similar to the traditional compressor, this compressor is



characterized by (4) to (7), which are the same. An adder function was reduced to two XOR gates and a 2- 1MUX, which were then placed in a way to reduce the critical path. It is because of this that four gate delays are needed to achieve the sum and carry outputs in this design.

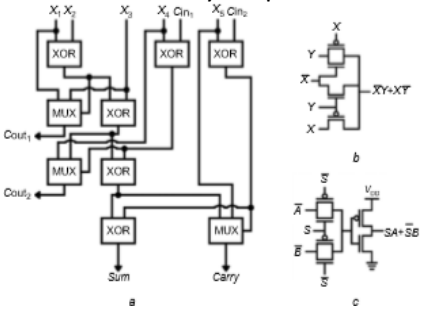


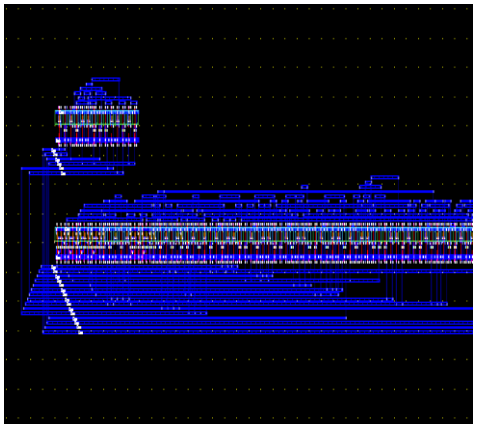
Fig. 2 Architecture of the proposed 5-2 compressoraBlockdiagram

b Schematic of 2-input XOR cellc Schematicof2-1 MUXcell

Figure 3 depicts the planned 5- 2 compressor's complete transistor-level architecture. No threshold drops occur in the intermediate nodes, and the output

nodes are fully restored thanks to the employment of full-swing transmission gate logic and static inverters. Voltage/process scaling and cascade are possible because of these characteristics. In addition, this design does not use sophisticated static CMOS gates or dual rail XOR-XNOR logic, which need the usage of additional transistors. Since it has 58 transistors, it is the lowest-reported for a 5- 2 compressor, according to the authors' best information. A 65 nm CMOS technology layout

implementation is depicted in Fig. 4. VDD = 1 volt, T = 70 degrees Celsius): average power dissipation of tested circuits For a period of 100



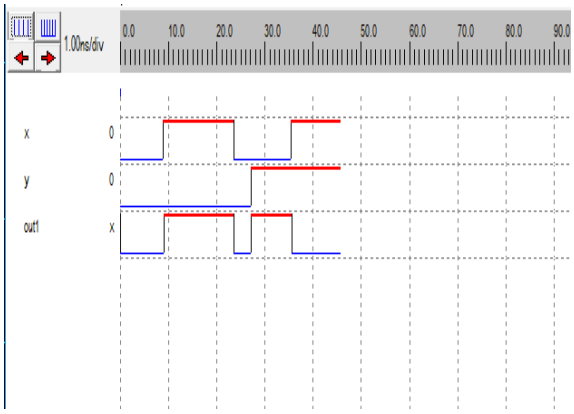
ns, the circuits were fed 1 GHz frequency input bit sequences with a 50% switching probability. Input buffer power consumption was not taken into consideration.

Fig.3Transistorlevelimplementationoftheproposed5-2 compressor

IV.RESULTS

The proposed low-power high-performance CMOS 5-2 comparator with 58 Transistors circuits designedusing65nmCMOSprocessinMICROWIND, the size of PMOS is triple that of theNMOS transistor size to achieve the best power anddelay performance. The simulations were done usingDSCH and MICROWIND with a power supply of1V.

Simulationresultanddigitalschematicofsomeofthecircuitsusing DSCH3.5toolare givenbelow.



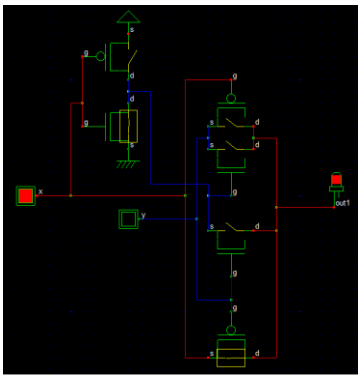


Fig4.Schematicof2 inputXORcellinDSCH

Fig5.Simulationresultof2inputXORcellinDSCH

Fig14.Layoutofproposed5-2compressorimplementedon65nmCMOS technology

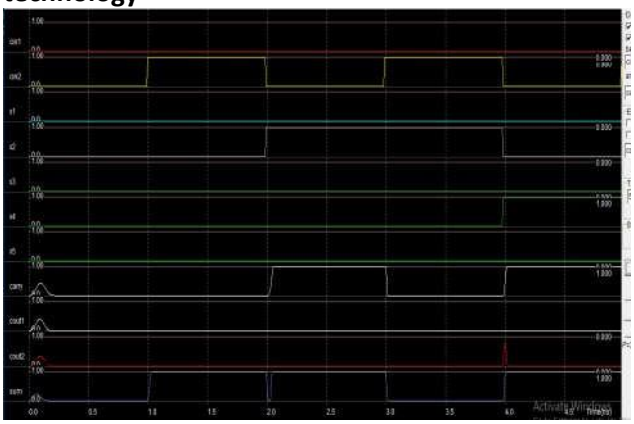


Fig13waveformofproposed5-2compressor

Table1: Comparison of5-2 compressors

Our CMOS 5-2 compressor design has the lowest documented device count of 58 transistors, and it is the first of its kind. It is possible to scale up and cascade the proposed circuit using full-swing logic and fully restored outputs. In addition, simulations show that it has the best overall power–delay performance among the designs that have been developed thus far. CMOSmultipliers with low power consumption and good performance can benefit greatly from the new 5-2 compressor, which has been found to be an effective part of the device.

References

[1].'Design of high-speed, low-power 3-2 counter and 4-2 compressor for rapid

multipliers', Electron Lett., 1998, 34 (4), pp. 341–343, doi:10.1049/el:19980306 [2]. As part of a 16-bit MAC design, Kwon, O.; Nowka, K. and Swartzlander, E.E. used the fast5:2 compression algorithm. IEEEInt.Conf.Application-Specific Systems, Architectures, and Processors, Boston, MA, USA, July 2000, pp. 235–243, doi:10.1109/ASAP.2000.862394. "

"Low-power 4-2and 5- 2compressors" by Prasad, K., andParhi, K.K.

An article published in the November 2001 issue of 35th Asilomar Conference on Signals Systems and Computers (ACSSC) in Pacific Grove, California provides an overview of the current state of the art in signal processing.

In 'Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for rapid arithmetic circuits,' Chang, C.H., Gu, J. and Zhang, M. published a paper in the journal Trans.

10.1109/TCSI.2004.835683

New architectures for high-speed and low-power 3-2, 4-2, and 5-2 compressors have been proposed by S. Veeramachaneni, K. M. Krishna, and L. Avinash, et al. An International Conference on VLSI Design was held in Bangalore, India in January 2007 and the following papers were presented: 10.1109/VLSID.2007.116

When it comes to quick arithmetic, the 5-2 compressor from Tohidi, Mousazadeh, Akbari, and coworkers is a godsend.

Proceedings of the 20th International Conference on the Mixed Design of Integrated Circuits and Systems in Gdynia, Poland, June 2013.

In 'High-speed energy-efficient 5:2 compressor,' Najafi, A., Timarchi, S., and Najafi, A. Information and Communication Technologies for Development (ICTD 37)

Proceedings of the 2014 International Conference on Microelectronics and Nanotechnology (MIPRO), Opatija, Croatia, May 2014.

'Low-power and high-performance 5:2 compressors' by Najafi, A., Najafi, A., and Mirzakuchaki, S. IAEA's 22nd International Conference on Electrical and Electronics Engineering (IACEE) was held at Tehran's Mehrabad International Airport in May 2014.

At http://ptm.asu.edu/, accessed August 2017, the University of California Berkeley provides a 'Predictive Technology Model (PTM)'.

Design Transistors Power