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Equal Segmentation based Approximate Adder Design for High Speed Operations

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Abstract: It's not always necessary to get the most accurate results in many cases, such as in image and multimedia data processing, artificial intelligence, and machine learning. As a result, approximation computing has been developed. Using approximation computing makes a big impact in terms of the amount of space, latency, and power used. It may not be the best choice for error-resistant applications since its ED is too high; and Error also rises as bandwidth increases. This research introduced a novel strategy that is equally segmented in order to enhance these parameters. Using this technique, an N-bit adder is broken down into equal-sized and accurate sub-adders. Segment size (k) is one of two factors used to build an N-bit ESA. Carry propagation length and Overlapping bits are two examples of this. It's the bare minimum in terms of carry prediction bits. So the best configurations differ depending on the ESA adder design. Three kinds of adder architectures are included in our analysis: those with smaller area; those with smaller delay; and those with an in-between delay and area size.

Keywords— A full adder is a kind of adder that divides a number into equal parts (ESA) (FA).

I.INTRODUCTION

One of the most important needs for electronic systems is to minimise energy consumption, particularly in portable devices like smartphones, tablets, and other gadgets. Those are sought after because of their limited speed. DSP blocks are essential building blocks for a wide range of applications. Additions and multiplications are the most important arithmetic blocks in the computing core. High energy and power consumption might result from the use of adders, which play an important part in processing. In order for a processor to be functional, it relies heavily on the amount of power and energy it uses.

Multimedia, wireless communication, recognition, and data mining are examples of applications that can tolerate certain faults. Errors do not affect image, audio, or video processing apps, such as Photoshop. In digital signal processing, there is a limit to the accuracy of the calculated outputs because of the noise in the input signals.

For the greatest possible expansion of the system's capabilities, many approximation adders have been given and examined. Shortening the carry chain in approximation adders is the primary circuit's purpose. The Equal Segment Adder and the Approximate Full Adder are two ways to divide the design. There are

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two sub-adders in the Approximate Full Adder approach. While the lower-order bits were seen as approximate adders, the higher-order bits were regarded as exact adders. An N-bit adder was broken into multiple smaller equal-sized sub-adders using the Equal segment adder technique. Carry in was regarded as a 0 for all Sub adders. As a result, each sub-adder is free to work on its own.

Other sections are laid out as follows. Section II depicts the work that was done in the past. Section III outlines the proposed approach to design. Section IV details an experiment and the findings it produced. Section V concludes the discussion of the work's influence.

II. EARLIER WORK

Digital systems can't function without adders. Data-heavy applications, such as multimedia, are best suited to digital systems. It has a longer delay than any other adder circuit, but it is the smallest in terms of both area and bit-width (O (N)). In computing, there are three primary error-resistant techniques: approximation, probabilistic, and stochastic. Approximate computing has garnered a lot when compared to other two methodologies. Approximate computing for research and practical purposes is the focus of this study.

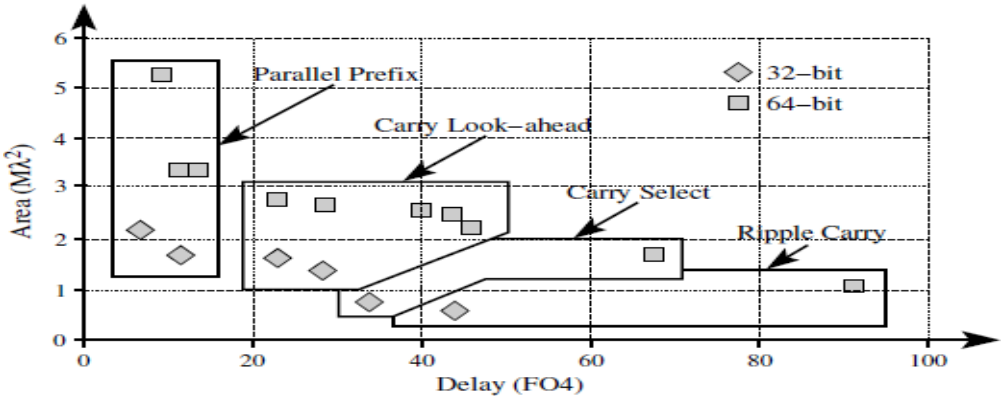

Fig.1 Delay versus area of conventional adder architectures

Various approximation adders have been utilised in the literature in recent years. The biggest problem is as the bit length of the adder rises, as stated in the preceding paragraphs. Carry propagation rises in tandem with bit length. As a result, there will be an increase in latency. Area, delay, and power were all considered while evaluating the effectiveness of previous techniques. We used the approximation approach, which was devised by dividing the adder into equal pieces, to enhance the evaluation parameters.

From a technological standpoint, AC plays a significant role in numerous applications. An approximation adder, which can execute the basic arithmetic operations in a digital system and the Delay power bottleneck, is of great relevance. In microarchitecture, adders may be a source of latency problems due to their high power consumption. The approximation adders are used to get around the digital system's power bottleneck.

Digital circuits are often assessed in terms of size, latency, and power consumption. Although latency, power, and area are all important parameters in approximation computing, accuracy is the most important. Quality measures like as Error Distance (ED) and Error Rate (ER) are often used to quantify the accuracy of approximation circuits (ER).

III. PROPOSED ADDER DESIGNS

Designing approximation adders with the use of the Equal Segment Adder (ESA) approach is common practise. In this work, we discuss the significance of the design methodology as well as some key performance indicators for ESAs in general. The ESAs are easier to grasp for newbies if they are presented in an organised manner. Because of this, we've developed various analytical methods for assessing

accuracy in terms of error distance, error rate, and mean square error. Delay, power, and area were used to describe the ESA setup. Figure 2 depicts the generalised architecture of an ESA-based n-bit approximation adder.

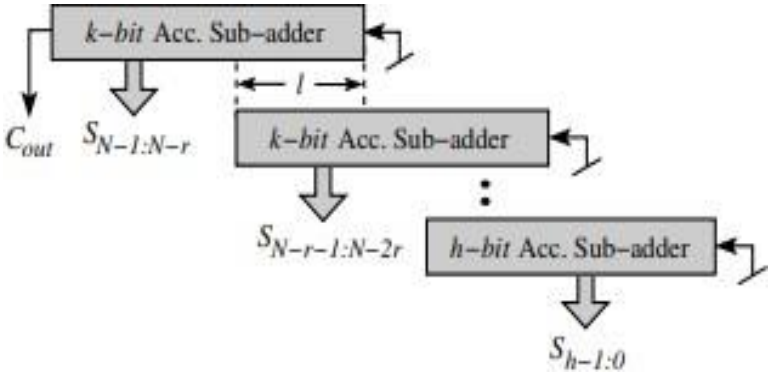

Fig.2 Generalized architecture of ESA based approximate adder

Overlapping bits or the minimum number of bits utilised in carry prediction should be in l k N, where N is the Segment size or the maximum length of carry propagation and it should be in the ranges of zero to l k. An expression for r may be found by writing r as the number of output bits per sub-adder that go into the final total. A sub-adder having a value of h that is the least significant.

$h = N - (k - l)($

$N - k$

$k - l$

For better performance evaluations, we are considering the overlap bit l as zero. From this modified structure the delay will be reduced. The modified structure of the equal segment adder is illustrated in Fig 3.

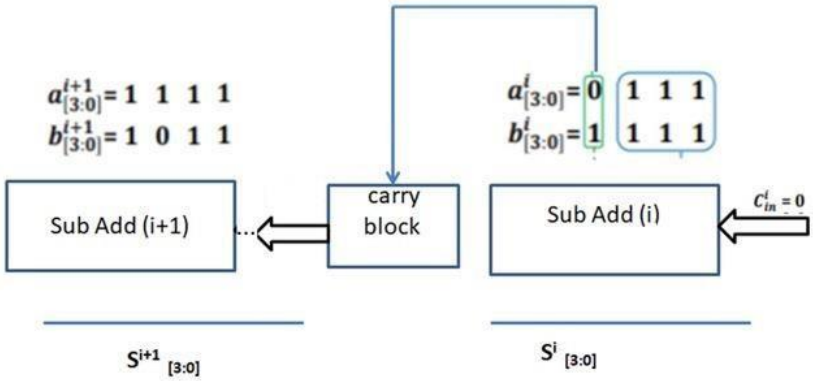

Fig 3: Proposed Equal segment adder structure

In the figure (3), I is the number of sub adders. By foreseeing the carry, the suggested design reduces latency. A and B may be used to indicate the projected carry.

Carry Increment Adder, Kogge Stone Adder, and Ripple Carry Adder are all used to implement the sub-adders. In comparison to ripple carry adder, carry look ahead adder, and kogge stone adder, ripple carry adder takes up less space and has a shorter lead time. MSE, ED were used to describe the degree of accuracy. Proposed research allows ESAs to be used more effectively.

IV. RESULTS & DISCUSSIONS

Xilinx 14.7 Verilog HDL tool may be used to simulate these tests. We are focused on the

addition technique in this study. For optimal digital circuit performance, the propagation delay must be as short as possible. Various adder topologies provide varying numbers of LUTs and delays for the Equal segment adder, as seen in the pictures below. According to the data, the Kogge stone adder outperforms all other algorithms tested in this study.

Table I: Comparison table for various adder architectures.

	CLA	RCA	KSA
Area (Lut's)	53	43	43
Delay(ns)	9.130	9.942	7.797

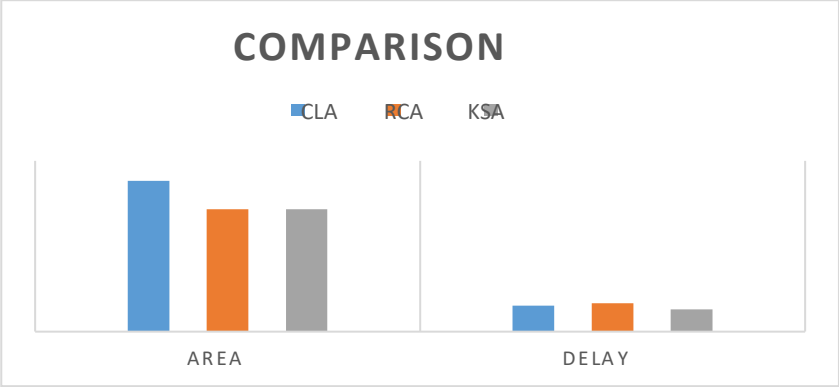

Fig 4: Comparison of various adders in terms of area and delay

Below mentioned figures are obtained after implementation where fig.5 represents the block diagram and fig 6. Represents the technology schematic of RCA which includes Look Up Table interconnections.

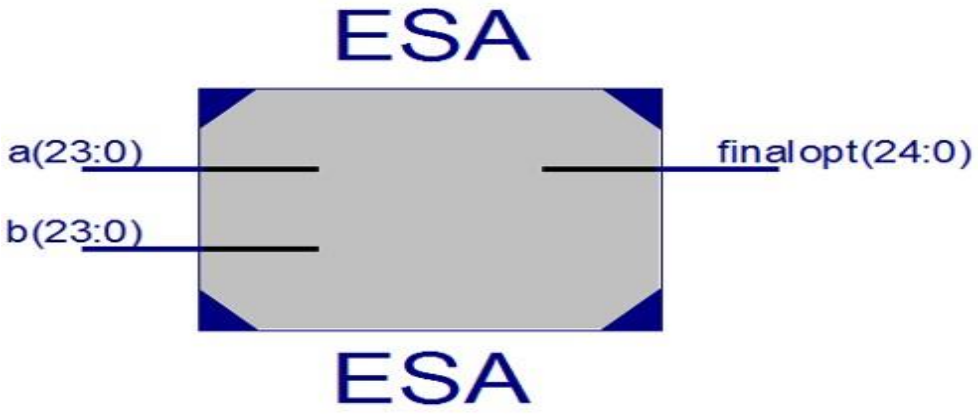

Fig 5: RTL schematic of RCA

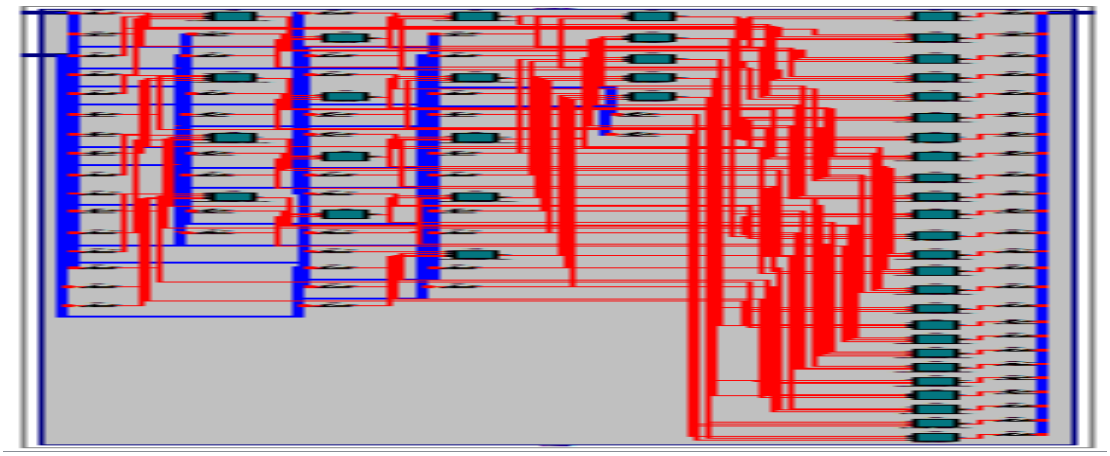

Fig 6: Technology schematic of RCA

V. **CONCLUSION**

When compared to other current adders, such as conventional and parallel prefix adders, we provide in this study an approximation adder with equal segment structure and accurate full and half adders. To achieve equal segmentation, all of the suggested adders are based on mean square error quality adders.

REFERENCES

1. First, N.Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, was published. Addison-Wesley Publishing Company, 2010 in the United States.
2. "Approximate Computing" by S. Mittal, "An Overview of Techniques," ACM Computing Surveys, Vol. 48, No. 4, March 2016, Pages 62:1–62:33.
3. This paper by K. Palem and A. Lingamneni is entitled "Ten Years of Building Broken Chips: The Physics and Engineering of Inexact Computing," and it was published in the May 2013 issue of ACM Trans.
4. For further information on stochastic computing, see Alaghi and Hayes, "Survey of Stochastic Computing."
5. N. Bombieri, M. Poncino and G. Pravadelli, Smart Systems Integration and Simulation, 1st ed., Springer Publishing Company, Inc. 2016.
6. "Dark Silicon and the End of Multicore Scaling," in 38th Annual International Symposium on Computer Architecture (ISCA), June 2011, p. 365–376.
7. DARPA/ISAT Workshop, March 2012. 7. M. D. Hill and C. Kozyrakis, "Advancing Computer Systems Without Technology Progress," in an ISAT outbrief.
8. Approximate Computing: Analysis and Characterization of Inherent Application Resilience, in 50th ACM/EDAC/IEEE Design Automation Conference (DAC), May 2013, pp. 1-9, Chippa, S. Chakradhar, K. Roy, and A. Raghunathan.